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DESIGN OF A LOW POWER DOUBLE TAIL COMPARATOR USING GATED CLOCK AND POWER GATING TECHNIQUES

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ABSTRACT

In this paper, performance of various types of dynamic double tail comparators (Gated clock and power gating technique) are compared in terms of their power, Delay, speed, Rise time, fall time, average time. The accuracy of comparators, which is defined by its power consumption and speed, is of keen interest in achieving overall higher performance of ADCs. In the domain of Signal processing with Low Power VLSI, the role of ADC system is essential. Many high speed ADCs, such as flash ADCs, require High speed, Low power comparators with small chip area. High-speed comparators suffer from low supply voltages especially when threshold voltage of the devices is not scaled at the same pace as the supply voltages of the modern CMOS process. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. . The maximum clock frequency of the proposed comparator can be 600GHz at supply voltages of 0.8 and 0.5 V, while consuming 111µw and 130 µW, respectively.

1. INTRODUCTION

Comparators have essential influence on the overall performance in high speed analog to digital convertors (ADCs). In wide-ranging a comparator is a device, which compares two currents or voltages and produces the digital output based on the comparison. Since comparators are usually not used with feedback, there is not a need for compensation so neither the area reduction or speed reduction value is invited. Comparators are known as 1-bit analog to digital converter and for that reason they are mostly used in large quantity in A/D converter Dynamic comparators are widely used in the design of high speed ADCs. Due to speed, low power consumption, high input impedance and fullswing output, dynamic latched comparators are very attractive for many applications such as high-speed analogto-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers.[1] High speed flash ADCs, need high speed, low power and small chip area. The designed dynamic latch comparator is required for high-speed analog-to-digital converters to get faster signal conversion and to reduce the power dissipation, which is protected to noise. However, since this comparator has two tail transistors which limit the total current flowing through the both of the output branches, it shows strong dependency on speed and offset voltage with different common-mode input voltage Vcom. To mitigate this drawback, the comparator with separated input-gain stage and output-latch stage was introduced. The structure of double-tail dynamic comparator is based on designing a separate input and cross coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range. The conventional double-tail comparator does not require boosted voltage or stacking of too many transistors. A conventional double-tail comparator has less stacking and then can activate at lower supply voltages compared to the conventional dynamic comparator. Basically by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This is also results in considerable power savings when compared to the conventional doubletail comparator. In this paper, a comprehensive analysis about the delay and power of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in, a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. The rest of this paper is organized as follows. Section 2 investigates the operation of the conventional double tail comparators and the pros and a con of each structure is discussed. Delay analysis is also presented and the analytical expressions for the delay of the comparators are derived. The proposed comparator is presented in Section 3. Section 4 Simulation results are addressed, followed by conclusions in Section 5.

2. CONVENTIONAL DOUBLE TAIL COMPARATOR

A conventional double-tail comparator is shown in Fig. 1. This comparator has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail make possible both a large current in the latching stage and wider Mtail2, for fast latching free of the input common-mode voltage (Vcm), and a

small current in the input stage (small Mtail1), for low offset . The operation of this comparator is as follows (see Fig. 4). During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an inputdependent differential voltage Vfn(p) will make up. The intermediate stage formed by MR1 and MR2 passes Vfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.

Despite the effectiveness of this idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [Msw1 and Msw2, as shown in Fig. 5(b)]. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

3. CONCLUSION

In this paper, a comprehensive delay analysis for double tail comparators is done. Two common structures of conventional double tail comparator and conventional double-tail dynamic comparators were analyzed. Analysis on delay, rise time, fall time, average delay time were done. A new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 125nm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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