



AREA AND POWER EFFICIENT OF PIPELINE VLSI ARCHITECTURE OF THE 2-D DWT

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ABSTRACT

Several techniques square measure accustomed scale back power dissipation by eliminating spurious transitions .Truncated multiplier factor is employed to scale back space and therefore the power dissipation of pipeline VLSI design of the second DWT and improve performance. The relationships that exist between the coefficients of the filters in varied sub bands may then be utilised to more enhance the in operation speed of the pipelines. In applications like video compression, medical imaging and geographic information analysis, it's 2-D wave transforms that square measure used.

1. INTRODUCTION

The 2-D separate wave transforms (DWT) are wide employed in several engineering applications owing to their multi-resolution decomposition capability[1]. However, process massive volumes of information of assorted decomposition levels of the rework makes their computation computationally terribly intensive. within the past, several architectures are planned aimed toward providing highspeed 2-D DWT computation with the need of utilizing an affordable quantity of hardware resources. These designs is broadly speaking classified into severable and nonseparable architectures[17]In a severable architecture, a 2-D filtering operation is split into 2 1-D filtering operations, one for process the datarow-wise and therefore the alternative columnwise.This design needs advanced management units to facilitate the interleaved operations of the output samples of various decomposition levels by using a algorithmic pyramid formula (RPA) . This will increase the memory size yet because the latency of the architectures. The non-separable architectures don't have this drawback, since in these architectures, the 2-D transforms square measure computed directly by mistreatment 2-D filters. Most existing nonseparable architectures aim at providing quick computation of the DWT by mistreatment pipeline structures and an oversized variety of parallel filters. However, these existing architectures haven't exploited the procedure [12] similarity inherent within the DWT operation to the extent doable so as to produce a high speed. The high-speed computation is achieved by with efficiency distributing the task of the computations of multiple decomposition levels among the stages alternative pipeline, and by optimally configuring the information and synchronizing the operations of pipeline thus on maximize the inter-stage and intra-stage procedure similarity.

2. FORMULATIONS FOR THE COMPUTATION OF THE 2-D DWT

The 2-D DWT is associate degree operation through that a 2-D signal is in turn rotten in a very spacial multiresolution domain by lowpass and highpass FIR filters on every of the 2 dimensions. The four FIR filters, denoted as highpass-highpass (HH), highpass-lowpass (HL), lowpass-highpass (LH) and lowpass-lowpass (LL) filters, produce, severally, the HH, HL, luteinizing hormone and LL subband information of the rotten signal at a given resolution level.[1] The samples of the four subbands of the rotten signal at every level square measure calculable by an element of 2 in every of the 2 dimensions. For the operation at the primary level of decomposition, the given 2-D signal is employed as input, whereas for the operations of the succeeding levels of decomposition, the decimated LL subband signal from the previous resolution level is employed as input. The four FIR filters use the truncated multiplier factor for multiplication method.

At any resolution level, the separation of the sub band process admire even and odd indexed information is according to the need of destruction of the information in every dimension by an element of 2 within the DWT computation[1]. it's conjointly seen from that the filtering operations within the four channels square measure freelance and identical, which might be exploited within the style of associate degree economical pipeline design for the 2-D DWT computation



3. SIMULATION RESULTS AND COMPARISONS

3.1 style of Stages

In the planned three-stage design, stages one and a couple of perform the computations of levels one and severally, and stage three that of all the remaining levels. Since the fundamental operation of computing every output sample, despite the decomposition level or the sub band, is that the same, the computation blocks within the 3 stages will disagree solely within the variety of identical process units used by them relying one quantity of the computations allotted to the stages. associate degree window of the raw 2-D or that of associate degree LLsub band data should be rotten into four distinct subwindows in accordance with the four rotten terms given by the correct facet of (4). This decomposition is accomplished by coming up with for every stage associate degree applicable information scanning unit (DSU) supported the method the raw input or the LL-sub band information is scanned[19]. The stages would conjointly need memory area (buffer) to store the raw place information or the LL-sub band information before scanning. Since stages and a couple of have to be compelled to store solely a part of many rows of raw input or LL-sub band information at a time, they need a buffer of size of, whereas since stage three must store the whole LL-sub band information of one decomposition level, it's a buffer of size of $O(N)$.

3.2 Structure of the information Scanning

Unit In accordance with associate degree window of the raw 2-D keep in or associate degree LL-subband data keep in or ust be partitioned off into four sub-windows, and keep into the DSU of the corresponding stage. Further, this same quation conjointly dictates that a 2-D input file should be scanned in a very serial manner shown in step with this sequence of scanning, the samples in a very set of information comprising rows of a 2-D input file square measure scanned ranging from the top-left corner. Once the scanning of all the samples of rows is completed, the method is recurrent for one more rows once shifting down by 2 row positions. the target is then to style a structure for a DSU so samples scanned with this serial mode get partitioned off into the four sub-windows so as to partition associate degree window into four sub-windows, the structure of the DSU should initial partition the samples of the window into 2 elements betting on whether or not a sample belongs to associate degree even-indexed or odd-indexed row.

3.3 Distribution of Filtering Among the process Units used by Stages

It moldering input file into four sub bands needs four filtering operations, and every of the four filtering operations needs four -tap filtering operations. Thus, a complete of sixteen -tap filtering operations square measure concerned for the computation of the samples for the four sub bands mistreatment associate degree window of the input file. Now, for every stage, these sixteen sorts of filtering operations should be allotted to the process units obtainable to the stage mistreatment four subwindows of information from its DSU. Given the obtainable resources of the stages, the target here is to method the sixteen sorts of filtering operations with maximized procedure similarity and with priority given to the computation of the samples of LL sub band.

In this figure, the four sub-windows, 1 to 4, square measure chosen in turn, as input to for every sub-window, the process unit then carries out the -tap filtering operations. during this stage, produces consecutive the LL, LH, HH and hectoliter subband samples in sixteen consecutive clock cycles. Note that one process unit at a time processes the samples of only 1 sub-window admire one in all the four subbands. Assume that such a time interval by a process unit to be just once unit. Now, since stages one, a pair of and three have eight, a pair of and one process units, severally, they'll method subwindows at the rates of two, 1/2 and 1/4 sub-windows per unit time. This as well as the very fact that the process hundreds (i.e., the quantity of sub-windows) allotted to the 3 stages square measure within the magnitude relation 8:2:1, lets United States to conclude that the operations of the 3 stages square measure reciprocally synchronised.

3.4 style of the process Unit

In every stage, a process unit carries out Truncated multiplier factor operation mistreatment the samples of associate degree sub-window at a time to supply the corresponding output. Since the subwindows can't be fed into a process unit at a rate quicker than the speed at that these sub-windows square measure processed by the process unit, the time interval to method a subwindow (one time unit) is crucial in determinative the most clock frequency at that the process units will operate. Therefore, it's crucial to aim at achieving the shortest doable delay for the crucial path once coming up with a process unit for our design. The filtering operation distributed by a process unit, as delineated higher than, is seen as parallel multiplications. The shortest crucial information path is achieved by minimizing the quantity partial product bits and/or the carry bits from completely different rows have to be compelled to be adscititious. this will be done by using in truncated multiplier factor.



4. CONCLUSION

Reducing the facility dissipation of parallel multipliers is vital within the style of digital signal process systems. In several of those systems, the merchandise of parallel multipliers square measure rounded to avoid growth in word size. the facility dissipation and space of rounded parallel multipliers is significantly reduced by a way called truncated multiplication. With this system, the smallest amount significant columns of the multiplication matrix aren't used. Instead, the carries generated by these columns square measure calculable. This estimate is adscitious with the foremost significant columns to supply the rounded product. The planned work is enforced in FIR filter structure, wherever the results of the FIR structure with mounted breadth multiplier factor show extended space reduction and therefore the power is additionally reduced.

5. FUTURE IMPROVEMENT

In the future work, varied techniques are developed to scale back the facility dissipation of parallel multipliers. many of those techniques scale back power dissipation by eliminating spurious transitions .Other analysis has centered on developing multiplier factor architectures and sign-extension techniques to scale back power dissipation and improve performance. The relationships that exist between the coefficients of the filters in varied sub and s may then be utilised to more enhance the in operation speed of the pipelines. In applications like video compression, medical imaging and geographic information analysis, it's 2-D wave transforms that square measure used.

REFERENCE

- [1] Chengjun Zhang, Chunyan Wang, "A Pipeline VLSI design for quick computation of the second separate wave Transform", Senior Member, IEEE, and M. Omair Ahmad, Fellow, IEEE, Transactions on circuits and systems-I, Vol. 59 NO eight Gregorian calendar month 2012
- [2] P. K. Meher, B. K. Mohanty, and J. C. Patra, "Hardware efficient systolic-like standard style for twodimensional separate wave rework," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 2, pp.151–155, Feb. 2008.
- [3] M. Ferretti and D. Rizzo, "Handling borders in beat architectures for the 1-D separate wave rework for good reconstruction," IEEE Trans. Signal method., vol. 48, no. 5, pp. 1365–1378, May 2000.
- [4] Q. Dai, X. Chen, and C. Lin, "A novel VLSI design for three-dimensional separate wave rework," IEEE Trans. Circuits Syst. Video Technol., vol. 14, no. 8, pp. 1105–1110, Aug. 2004
- [5] J. Song and I. Park, "Pipelined separate wave rework design scanning twin lines," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 12, pp. 916–920, Dec. 2009.
- [6] M. Ravasi, L. Tenze, and M. Mattavelli, "A scalable and programmable design for 2-D DWT cryptography," IEEE Trans. Circuits Syst. Video Technol., vol. 12, no. 8, pp. 671–677, Aug. 2002.
- [7] K. C. Hung, Y. S. Hung, and Y. J. Huang, "A nonseparable VLSI design for two-dimensional separate periodized wave rework," IEEE Trans. terribly massive Scale Integr. (VLSI) Syst., vol. 9, no. 5, pp.565– 576, Oct. 2001.
- [8] K. G. Oweiss, A. Mason, Y. Suhail, A. M. Kamboh, and K. E. Thomson, "A scalable wave rework VLSI design for period of time signal process in highdensity intra-cortical implants," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 6, pp.1266–1278, Jun. 2007.
- [9] C. Cheng and K. K. Parhi, "High-speed VLSI implementation of 2-D separate wave rework," IEEE Trans. Signal method., vol. 56, no.1, pp. 393–403, Jan. 2008. S. Masud and J. V. McCanny, "Reusable Si information science cores for separate wave rework applications," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 51, no. 6, pp. 1114–1124, Jun. 2004.
- [10] K. A. Kotteri, S. Barua, A. E. Bell, and J. E. Carletta, "A comparison of hardware implementations of the biorthogonal 9/7 DWT: Convolution versus lifting," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 52, no.5, pp. 256–260, May 2006.