Comparsion of Performance Parameters of CNTFET Based 3Value Logic Memory cell and CNTFET Based 6T SRAM Using HSPICE

S.Tamil Selvan 1 Dr. M.Sundarajan 2

1 Research scholar, Bharath University, chennai, TamilNadu
2 Principal at Alpha College Engineering and Technology Pondicherry

ABSTRACT
This paper presents a design of a 3ValueLogic memory cell using carbon nano-tube field-effect transistors (CNTFETs). 3VL is a promising alternative to conventional binary logic, as it has better performance in terms of low power and also reduces propagation delay. This cell uses a control gate for the write and read operation to make them separate. Transmission gate is used as control gate in this circuit. The CNTFET used for design has different threshold voltages to achieve ternary logic. This multi threshold voltage is obtained by varying the diameter of the CNT used. Chirality of the CNTFETs is utilized for varying the diameter of the CNT and it also avoids the usage of additional power supplies. The channel length used here is 32nm wide. The power consumption is reduced as there is absence of stand-by power dissipation. Second order effects are removed by using CNTFET in the circuit. The two memory operations, bit read and bit write operation of the 3ValueLogic cell perform correctly at 0.9V power supply. In a3Value Logic, it only takes log3 (2n) bits to represent an n-bit binary number. The various performance parameters of 3VL memory cell and 6T SRAM CNTFET measured using HSPICE

Keywords: CNTFET, 3ValueLogic, HSPICE, Multi threshold value, FINFET, QDGFET, SNM

1. INTRODUCTION
A one-bit memory cell is a basic building block of designing array of memory structure and for huge storage memory devices. There are two operations are to be performed in memory cell, they are read operation and write operation. The read operation is to obtain a data value from the cell, write operation is to store a data in to the memory cell. One-bit memory cell can be either latch or flip flop. This memory cell can be for designing SRAM, DRAM, PROM, Mass storage like hard disk, flash memory, memory cards etc. They can be even used in microprocessors and in microcontrollers as ROM array and RAM cells of required size. The access time to the memory cell must be faster and should consume less power. Traditionally, memory cell was designed with binary logic using MOSFET with CMOS technology. The miniaturization of electronic components has been a great deal towards the VLSI industries which give rise to many advanced FETs and efficient logic design. The key features of these advancements in FETs are designing low power, high speed digital circuits. The advanced FETs are FinFET, CNTFET, QDGFET, SET etc and efficient logics are reversible logic, multi-value logic, and adiabatic logic. The memory cell is designed with CNTFET using ternary logic, which is part of multi-value logic. Ternary logic is also known as 3-value logic. The carbon nanotube field-effect transistor (CNTFET) is a rising technology to a well known bulk MOSFET for low-power and high-performance designs due to the realistic transport [4]–[6]. In a CNTFET, the threshold voltage is determined by chirality factor and hence the diameter, so a multi-threshold design can be consummated by using CNTs with different diameters in a CNTFET. The design of a 3value logic family using CNTFETs has been contemplated in [7]; a basic 3 value gates has been presented. 3 value arithmetic circuits such as a full adder and multiplier have been contemplated as examples of the application of a 3value gate technique. Simulation results have confirmed [7] that significant power and delay advancements are possible by utilizing this 3 value logic family at both gate and circuit levels. It is said that a design methodology using the CNTFET-based 3 value logic is a feasible solution for low power and high performance VLSI circuit design in the submicron nano ranges[7]. Our goal is to design promising memory cell with CNTFET using 3 value logic which can perform both read and write operation with low power consumption and high switching speed. Large amount of data can be stored in minimum chip area. A carbon nano-tube (CNT) is an excavated cylinder comprises of one or more layers of graphene atoms arranged in a hexagonal network structure. A CNT with many layers is called as multi-wall CNT and a CNT with simple singular layer of carbon atoms is called a single-wall CNT. A single-wall CNT can act as either a metal or a semiconductor; build upon on the angle of the
atomic arrangement along the CNT. Multi-wall CNT mostly exhibits conducting behavior because of the increased clusters carbon atoms around them having a conducting shell. Many using semiconducting SWCNTs to design electron devices contradictory to MOSFETs; these devices are known as CNTFETs, also called TUBEFETs. CNTFETs are promising nanoscale devices for designing high-performance circuits. A recursive algorithm iteratively uses integration to find the so-called self-consistent potential. This significantly reduces performance. Semi- empirical models rely on curve fitting. When a parameter changes, a new fit must be determined in order to obtain the updated model. This is time consuming and complex for a large circuit in which parameters change for many devices. In this article, is address these problems with a computationally efficient circuit-level model of a CNTFET’s drain-source current. The ternary cell utilizes the chirality feature of CNTFETs for threshold voltage control, such that there is no need to provide additional power supply levels for ternary operation. The separate features of the proposed circuit for the write and read operations make this design very efficient. The rest of this paper is organized as follows. Section II starts with carbon nanotube transistors, followed by the SRAM design Using CNTFET is evaluated with respect to the write and read operations in Section III, the 3VL logic design is Section IV 3 value logic memory cells is then proposed, analyzed, and evaluated with respect to the write and read operations in Section V. Traditional performance measures for a memory cell design, such as power and delay are simulated by HSPICE in Section IV, conclusion in Section VII.

2. CARBON NANOTUBE FIELD-EFFECT TRANSISTOR
Carbon Nano-Tube Field Effect Transistor(CNTFET) is one of the advanced FET technology in the VLSI industry. The remarkable electrical properties of carbon nano-tubes arise from the unified electronic network structure of graphene itself that can binded up and form a excavated cylinder. The CNT is connected between source and drain regions as in the MOSFET device. The diameter of such carbon nano-tube can be expressed in terms of a chirality vector, which connects two crystallo-graphically equivalent sites of the two-dimensional graphene sheet. Here  and  are integers representing the hexagonal lattice. This structure can be described by an index with a pair of integers (, ) that define its chirality vector. An SWCNT can act as either a conductor or a semiconductor, depending on the dimension of the atomic alignment along the tube. In terms of the integers (, ), the nanotube diameter

\[
D_t = \frac{\sqrt{3}a_0}{\pi} \sqrt{m^2 + mn + n^2}
\]

where  is the inter-molecular distance between each carbon atom and another adjacent atom. Fig. 1 shows the schematic diagram of a CNTFET [9]–[11]. Similar to a conventional MOSFET device, we have four terminals in CNTFET. As shown in Fig. 1, lightly doped semiconducting nano tubes are placed under the gate region which is insulator when unbiased, and heavily doped CNT segments are placed at the either end of the drain and source side to allow for a low series resistance in the ON-state [4]. As the gate potential increases, the device is electro statically turned ON or OFF, with the help of gate. In the last decade two different CNTFET circuit design techniques have been used in the literature. One of them is directly replacing the MOSFET with CNTFET to approach better performance; The second is used CNTFET as a particular nanotechnology devices with its powerful CNT characteristics [8]. Fig.1 shows the schematic diagram of CNTFET. Transistors which use SWCNT have many benefits rather than silicon MOSFET counterpart such as high density of on current and moderately high Ion/Ioff ratio that has many effects on transistors behavior, molecular size, high theoretical transition frequency and changeable threshold voltage depending on carbon nanotube diameter which is an important characteristic of CNTFETs.

Fig.1. Schematic Diagram of CNTFET

The threshold voltage is defined as the minimum voltage required to turn ON the transistor; the threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half-band gap that is an inverse function of the diameter [9]–[11]:

\[
V_{th} = \frac{kT}{q} \ln \left(\frac{I_{ON}}{I_{OFF}}\right)
\]
\[ V_{\text{th}} \approx \frac{E_T}{2e} = \frac{\sqrt{3}}{3} \frac{eV_B}{D_c} \]  

(2)

where \( a = 2.49 \, \text{Å} \) is the carbon to carbon atom distance, \( V_B \) 
3.03 eV is the carbon \( \pi-\pi \) bond energy in the tight bonding model, \( e \) is the unit electron charge, and \( D_c \) is the CNT diameter. As the diameter of CNT changes, the threshold voltage of the CNTFET will also change. Assume that \( m \) in the chirality vector is always zero; then, the ratio of the threshold voltages of two CNTFETs with different chirality vectors is given as

\[ \frac{V_{\text{th}1}}{V_{\text{th}2}} = \frac{D_{c1}}{D_{c2}} = \frac{n_1}{n_3} \]  

(3)

Equation (3) shows that the threshold voltage of a CNTFET is inversely proportional to the diameter of the CNTs. For example, the threshold voltage of a CNTFET using \((13, 0)\) CNTs is 0.428 V, compared to a \((19, 0)\) CNTFET with a threshold voltage of 0.293 V. CNTFETs provide a ideal characteristics during the read operation. In 

3. SRAM DESIGN USING CNTFET

the 6T SRAM cell of Fig. 2 is designed using CNTFETs and its performance is assessed comprehensively with a newly proposed figure-of-merit denotes as “SPR” to compare stability, power dissipation, and write time with other existing SRAM cell designs. The basic design concept of the CNTFET-based memory has been proposed in [13] by the same research group, and this paper presents the actual design of the concept addressing the realistic design challenges and issues such as performance, Static Noise Margin (SNM), power consumption, and tolerance to PVT variations.

Read Operation

Prior to the read operation, BL and BLB of Fig. 2 are precharged to high level. When the wordline signal WL is high, the access transistors MN1 and MN2 are turned on, and the data stored in the SRAM is read. However, a read-upset problem is present during the read operation, and this may change the data stored in the SRAM cell. The read-upset problem can be described as follows. Assume that the cell is currently storing “1” so that \( q \) is “1” and \( n_q \) is “0”. When WL is high, MN1 and MN2 are on and the voltage at node \( n_q \) will rise. An appropriate sizing ratio between MN4 and MN2 is required to limit the voltage at node \( n_q \) to be higher than \( V_{\text{th}} \) such that the stored logic value does not change during the read operation. In the traditional CMOS design, the \( MN4/MN2 \) ratio should be greater than 1.28 for this requirement [12]. For the CNTFET SRAM design, simulations have been performed to establish the sizing ratio of MN4 and MN2. The gate and source of MN2 are connected to \( V_{\text{dd}} \) and the gate of MN4 is also connected to \( V_{\text{dd}} \) as the voltage at \( q \) needs to be set to “1”. The simulation results are shown in Fig. 6 for various \( MN4/MN2 \) ratios and gate lengths. The transistor size ratio of the two CNTFETs is measured as the number of tubes in the two CNTFETs unlike MOSFET. As mentioned in Section II, the threshold voltage of the \((19, 0)\) CNTFET is 0.289 V. Therefore, the \( MN4/MN2 \) ratio should be kept greater than 0.5 to keep the voltage of \( n_q \) below threshold voltage. However, for fair comparisons, the \( MN4/MN2 \) ratio used in this paper for the CNTFET SRAM design needs to be greater than 1.4 to control the low state voltage below the threshold voltage of the 32nm MOSFET which is 0.18 V [16].
Write Operation

During the write operation, the wordline WL is high to allow the data on bitlines BL and BLB to be written into the SRAM cell. For a successful write to a SRAM cell, the pull up transistor should not be too strong. Assume that the SRAM cell is storing “1” and it is required to write a new data “0” into the SRAM cell. The node q in Fig. 2 is going to be low, so the pass gate MN1 must be significantly more conductive than the PMOS MP5. In the traditional CMOS design, the MP5/MN1 ratio should not be greater than 1.6 [12]. For CNTFET SRAM design, simulations have been performed to establish the size ratio between MP5 and MN1. The bias voltage on the gate of MP5 is kept below Vds, and the bias voltage on the gate of MN1 is Vdd. Fig.3 shows the simulation results for various ratios and channel lengths. Any MP5/MN1 ratio of less than 1.6 can pull node q below 0.289 V, which is the threshold voltage of a CNTFET with (19, 0) nanotubes. Similarly to the read operation, the MP5/MN1 ratio used in this paper for the CNTFET SRAM design needs to be less than 1 to ensure that the write voltage at node q is not higher than the threshold voltage of the 32nm MOSFET (i.e. 0.1V). Therefore, for the proposed dual-diameter CNTFET-based SRAM cell design, the transistor size ratios among the pull up FET, the pull down FET, and the access transistors are MP5/MN1 = 0.5 and MN4/MN2 = 1.5. P-type CNTFETs with one tube are used for MP5 and MP6, while n-type CNTFETs with three tubes are used for MN3 and MN4. The number of tubes used for MN1 and MN2 is two. As the distance between two adjacent tubes within the same device is 20nm and the channel length chosen in this paper (as per previous discussion) is also 20nm [6], the dimensions of the pull-up transistor MP5, the pull-down transistor MN3, and the pass gate transistor MN1 are 40/20nm, 80/20nm, and 60/20nm, respectively (40/20nm denotes the width to length ratio). For a CMOS SRAM cell with a transistor length of 32nm and similar circuit performance to the CNTFET SRAM cell proposed in this section, the widths of MP5, MN3, and MN1 are found to be 80nm, 160nm, and 120nm, respectively. Therefore, there are two 80/32nm PMOS transistors, two 160/32nm NMOS transistors and two 120/32nm NMOS transistors in the CMOS SRAM cell. Compared to the CMOS 32nm feature size, the CNTFET-based SRAM cell has two 40/20nm P-CNTFETs, two 80/20nm N-CNTFETs, and two 60/20nm N-CNTFETs. These transistors are used in the next section to establish the best operation under the optimized threshold voltages for the dual-diameter CNTFET-based SRAM cell.

4. THREE VALUE LOGIC DESIGN

A three-value logic system was first developed by Jan Lukasiewicz, in 1920, in its popular paper O Logice Trójwarkosciowj, [12], as abstraction of the traditional binary logic. Three-value logic system has better characteristic compared to previous binary system such as increased bit handling capability per unit area, reduced number and complexity of interconnections, as well as reduced number of active FETs inside a chip. Hence, in the circuit which designs base on three-valued logic, circuits will be simpler and more flexible also more easy. By using 3VL higher speed and less power dissipation will be achieved [13] [14]. To obtain 3value logic system we need three values, in conventional binary system we have two logics values ‘0’ and ‘1’, these logics represented by 0V and Vdd respectively. In principle, 3VL can provide a means of increasing data processing capability per unit chip area. The serial and serial-parallel arithmetic functions can be carried out faster if the 3value logic is employed. One of the main merit of 3value logic is that it reduces the number of required computation steps. As each input can have three distinct values, the number of digits required in a 3VL family is log3 2 times less than that required in binary logic. It is assumed that
3-value logic elements can operate at a speed approaching that of the corresponding binary-logic elements. However, if the 3VL and binary logic gates are used to take advantage of their respective merits, performance could be significantly improved because 3-value logic gates are good candidates for decoding blocks since it requires less number of gates while binary logic gates are a good candidate for fast computational modules. Thus, 3-value design technique combined with the conventional binary logic design technique also provides an excellent speed and power consumption characteristics in memory circuits. Three value logic functions are defined as the functions having convincing if a third value is introduced into the binary logic. Here, 2, 1, and 0 denote the 3 logic values to represent true, intermediate, and false, respectively. Any n-variable \(\{Z_1, \ldots, Z_n\}\) 3 value logic function \(f(Z)\) is defined as a logic function mapping \(\{0,1,2\}\) to \(\{0,1,2\}\), where \(Z = \{Z_1, \ldots, Z_n\}\). The basic operations of 3-value logic can be defined as follows, where \(Z_i, Z_j \in \{0,1,2\}\)

\[
\begin{align*}
Z_i | Z_j &= \max\{Z_i, Z_j\} \\
Z_i \& Z_j &= \min\{Z_i, Z_j\} \\
Z_i &= 2 - Z_i
\end{align*}
\]

where “−” denotes the arithmetic subtraction, the operations “|,” “&,” and “−” are referred to as the OR, AND, and NOT in 3-value logic, respectively. The 3 value logic gates are designed according to the convention defined in above equation. Here work the set \{0, 1, 2\} is used, where 0 = false, 1 = intermediate, and 2 = true. Table 1 shows the truth table of all the basic 3-value logic gates. The choice of these values leads in a more natural way the adaptation of the ideas from the binary logic.

**Table 1** TRUTH TABLE FOR 3 VALUE LOGIC GATES

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>(Z = \text{NOT}(X))</th>
<th>(Z = \text{NOT}(Y))</th>
<th>(Z = X \text{ (OR) } Y)</th>
<th>(Z = X \text{ (AND) } Y)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
<td>2</td>
<td>0</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The 6T STI consists of six CNTFETs, in which there are three N-CNTFET Q1, Q2, Q3 and three P-CNTFET Q4, Q5, Q6. The chiralities of the CNTs used in (Q1, Q5) and (Q2, Q6) and (Q3, Q4) are (19, 0), (10, 0), and (13, 0), respectively. Their diameters of Q1, Q2, and Q3 are 1.487, 0.783, and 1.018 nm, respectively. Hence, the threshold voltages of Q1, Q2, and Q3 are 0.289, 0.559, and 0.428 V, respectively. The threshold voltages of Q5, Q6, and Q4 are −0.289, −0.459, and −0.328 V, respectively. When the input voltage changes from low to high at the power supply voltage of 1V, At the start, the input voltage is lower than 300 mV. This makes both Q5 and Q6 turn ON, both Q1 and Q2 turn OFF, and the output voltage 1V, which is logic 2. As the input voltage increases beyond 300mV, T6 is OFF and T5 is still ON. Where, Q1 is ON and Q2 is OFF. Once the input voltage exceeds 0.6 V, both Q5 and Q6 are OFF, and Q2 is ON to pull the output voltage down to zero. The input voltage transition from high to intermediate and then to low transition is similar to the low to intermediate then to high transition. This 6T- STI is used in most of the digital design based on the logic used. Other logic gates like NOR, NAND gates can be designed using this ternary logic. The main requirement of ternary logic is multi-threshold voltage FET devices.

![Fig. 4. Transistor level logic diagram of 6T STI](image-url)
5. 3VL Memory Cell Design

The memory cell is used to store one bit in it for the same time period until next write operation is performed. The read operation will not affect the value stored in the circuit. The memory cell is the basic storage unit in all semiconductor memories like RAM, ROM, Flash memories. The simple memory was constructed with back to back inverters are used in traditional memory cells as basic components of the storage element for the correct states; access transistors (such as pass or transmission gates) are commonly used to read and write from the back to back inverters. The design requirement for a memory cell is usually specified as follows: when the cell is holding the data (i.e., the access transistors are OFF), the cross coupled inverters must be able to hold the bi-stable states; when the cell is ready to write or read (i.e., the access transistors are ON), then the access transistors must be able to update the correct state. The traditional CMOS cell in a binary memory system uses six transistors (6T); two NMOS access transistors and two back to back CMOS inverters. The STI shown in Fig. 2 can be used as a basic storage element of the ternary memory cell. For the read and write operations, single-ended read and write access mechanisms are used. There must be a delay between read and write operation to avoid error of misread in the circuit.

6. Evaluation

SPICE simulation software is used write and read operation. The write transmission gate Q1 and Q2 allows the correct data from data in to wbl to be written into the memory cell q and qb. The read operation of the proposed ternary cell is performed as follows: rbl is pre-charged to 1/2 Vdd prior to the read operation and the read transmission gates Q17 and Q18 are accessed to read the correct data from the memory cell. The read operation of the proposed ternary memory cell has been simulated which operates as the ternary memory cell is storing a logic “2”; then, the read bit line rbl is charged to logic “2” when the read word lines rwl and rwlb are accessed. The ternary memory cell is storing a logic “0”; the read bit line rbl is discharged to logic “0” when the read word lines rwl and rwlb are accessed.

The ternary memory cell is storing logic “1”; rbl remains at logic “1”. A ternary STI is then connected to the read bit line rbl to sense the voltage at rbl. The average power consumption is measured using HSPICE for the proposed memory cell design. The power consumption is reduced due to usage of ternary logic with CNTFET. Compared to the high-leakage nano-CMOS device, a CNTFET has a significantly smaller OFF current; so, the power consumed when the transistor is OFF is greatly reduced in CNTFET designs. The CNTFET has a significantly higher ON-OFF current ratio compared to the MOSFET in the deep sub-micrometer range. The propagation delay is also reduced when compared to MOSFET circuits. For MOSFET CMOS circuits the minimum distance between pull up and pull down network must be 10 λ, but with CNTFET CMOS circuit the same must be 3λ so the area can be reduced though the no. of transistors increases.[21] Table 3 shows the power consumption and propagation delay of various Memory cells.
TABLE 3 RESULT COMPARISON OF VARIOUS PERFORMANCE PARAMETERS OF MEMORY CELLS

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>CNTFET 32nm 3VL Memory Cell</th>
<th>CNTFET 32nm 6T SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER</td>
<td>13.5 µW</td>
<td>14.2 µW</td>
</tr>
<tr>
<td>PROPAGATION DELAY</td>
<td>9.63ns</td>
<td>9.98ns</td>
</tr>
<tr>
<td>SNM (Volts)</td>
<td>0.21</td>
<td>0.26</td>
</tr>
<tr>
<td>WRITE MARGIN(V)</td>
<td>0.288</td>
<td>0.293</td>
</tr>
</tbody>
</table>

7. CONCLUSION

The 3VL 6T STI is designed with 32 nm technology and their parameters are analyzed. With the 6T STI CNTFET One bit memory cell is designed using 6T CNTFET SRAM and parameters are compared with 32nm 3VL CNTFET SRAM. It is found that the power consumed by 32nm CNTFET 3VL memory is 13.5 µW, which is much less than that of 6T STI CNTFET SRAM and other memory cell. All together the memory cell with 32nm CNTFET is considered as the most power efficient technology among the others. Thus as the channel length reduces the power consumption is also reduced. The future work consists of designing the memory with 18nm CNTFET technology, Cross bar memories with 18nm CNTFET has interesting applications.

REFERENCES


AUTHOR

Er S.TAMIL SELVAN pursuing Ph.D. in Bharath University. He has received the MTech degree in VLSI Design from Sathyabama University in 2011. He is currently working as HOD, Department of Electronics and Communication Engineering, Sri Krishna College of Engineering, Arakonam. Previously was working as Asst Professor in SMK Fomra Institute of Technology and as lecturer in KCG College of technology in Chennai. And he published various journal and international journals papers, His main research interests are in High speed digital VLSI circuits, Low power, Area reduction, synthesis and Simulation of digital circuits and FPGA Implementation

Dr. M.Sundarajan received his doctor degree in ECE from Bharath University, Chennai. Currently working as principal in Alpha College of engineering and technology Pondicheery. Previously was working as principal in Sri Lakshmi Ammal Engineering College, Gojan school of business and technology in Chennai. He published various international and national conference and international and national journal papers. Area of interest are Low power VLSI design circuits and digital image Processing